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Content

Simplified Calculation of DC-Link Capacitors for Automotive High-Performance xEV power train architecture

A capacitor in the intermediate circuit of the automotive inverter for storing and buffering energy is called DC Link capacitor (outlined in green in Figure 1). The main target of the DC Link capacitor with his capacitance is to absorb sufficiently current ripple generated by the fast switching 3 phase inverter power stage, which is connected to the motor through short cabling or bus bars.

*By Dipl.-Ing. Wolfgang Rambow, Rambow-Technology,
and Katharina Mankel, R&D, Mankel Engineering*

The capacitance is therefore chosen in order to keep the maximum DC-Link voltage ripple under control and at the same time to improve system energy density. These capacitors typically operate at high voltages extending from 400 V_{DC} to 800 V_{DC}. The automotive industry is well known for stipulating components that guarantee outstanding reliability when operating under influence of heavy stress, e.g. at extremely high temperatures, vibration and humidity. It is true, for all inverters, that the DC-Link capacitor, as an A-Component, is key to the design, reliability and, hence, its success. There is a large number of more or less complicated calculation formulas for DC-Link capacitance in PWM (Pulse Width Modulation - Figure 2) modulated inverters of electric cars available. Here we will show a simplified way to quickly find a pragmatic solution.

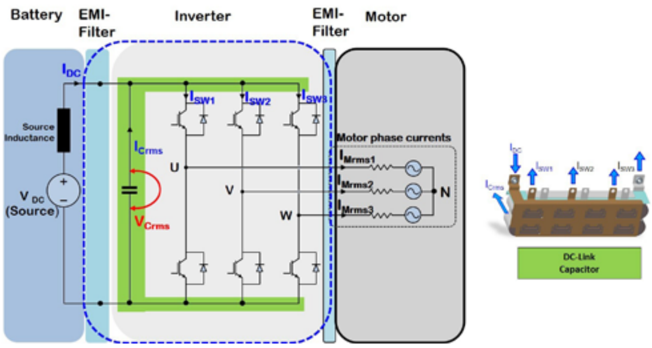

Figure 1: Simplified Power Train Circuit Diagram schematic and a Capacitors currents flow example [Source: Rambow Technology]

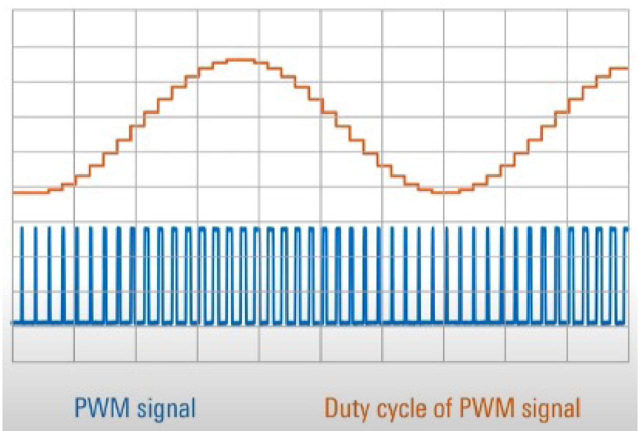

Figure 2: PWM - the duty cycle is being varied in a sinusoidal manner [3 source: Rohde&Schwarz]

In automotive power trains, the DC-Link film capacitor is mounted directly to single switches or semiconductor power module(s) (if B6 or half bridges are used) with very low ESL and ESR values (green colored in Figure 1). The vicinity of the capacitor to the power module is one essential target to minimize stray inductance between the power stage and the capacitor itself.

Applying an overlapping busbar concept keeps the ESL as low as possible while the ESR is determined by the inner construction of the capacitor itself. Even a few nanohenries of stray inductance in the capacitor current path raises the impedance at the switching frequency to levels that negate their effectiveness. Large ripple voltage indicate large ripple current flowing in bulk capacitors and can cause excessive power dissipation in the ESR. Before becoming thermally limiting, the proper selection of a capacitor and its location can have positive effects on the car's EMC robustness. If ripple voltages and corresponding currents kept low, the potential influence to safety relevant systems in the car is drastically reduced too, so that no interference occurs in the vehicle electrical system that could affect other functional modules.

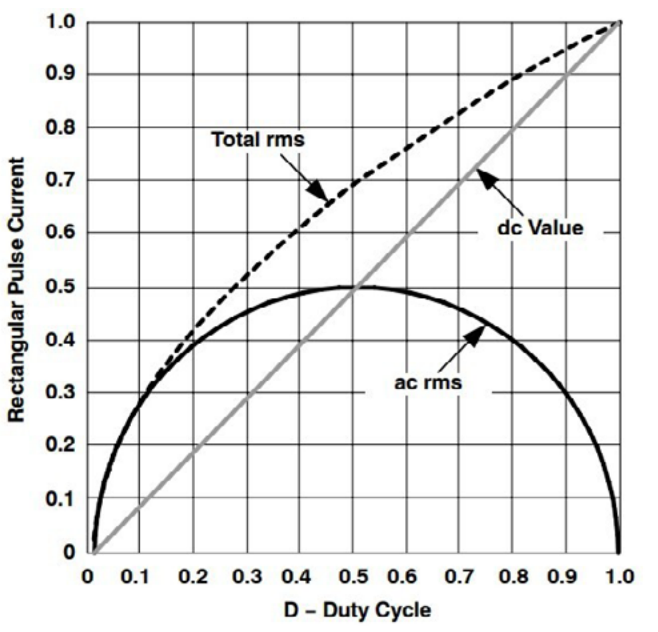

Figure 3: Magnitude drops on either side of 50% [1 Source: Texas Instruments]

As frequency goes up, the battery and cable parasitic source Inductance cause the impedance to increase. The DC-link capacitor impedance goes down so it becomes the preferable path for high frequency AC to circulate - capacitor ripple current (I_{Crms}).

Load current (I_{Mrms}) magnitude and the resulting capacitor ripple current (I_{Crms}), duty cycle (dc or m; in worst-case m=0.5), switching frequency (f) and temperature ($T_{(C)}$) are typical factors which determine the magnitude of the ripple voltage across the capacitors terminals. Since the ripple voltage amplitude is directly proportional to the output load current, the maximum current ripple amplitude occurs at maximum output load, which is not really surprising. The solid curve in figure 3 shows the calculated AC rms ripple amplitude that generates the considered loss in the capacitor. It reaches a maximum at 50% duty cycle. The chart [1 Source: TI] shows how this magnitude falls off on either side of 50%.

Various types of capacitor constructions can impact the considered capacitance. While classical high capacitive electrolytic capacitors do not play a major role in this application segment, the technology of power film capacitors come into focus – for good reason. Indeed Power film capacitor technology brings certain valuable advantages into designs, including:

- low DF (Dissipation Factor) = low ESR = low losses
- high current ripple current capability
- dry construction = no concern for evaporation
- selfhealing within limits

Some Key Design Considerations for Power Film DCLink Capacitors

Temperature robustness
The maximum hot spot temperature inside of each film capacitor elements is limited to 105°C (for polypropylene film, which is widely used). While the maximum self-heating temperature of the capacitor is 20°C, the heatsink temperature should not exceed 85°C. There are already film materials for 125°C available but cost as well as size makes them unattractive and in practice do not provide a better technological commercial match. Therefore, the cooling situation must be validated. Any excess of the maximum temperature of 105°C inside each of the capacitor elements will cause damage and will significantly reduce its lifetime. You can measure the hot spot temperature in the middle of the capacitors surface, if accessible. The result comes close to the existing temperature inside because most of these DC-Link capacitors are bulky and the temperature rises very slowly compared to semiconductors. Nevertheless, the DC-Link capacitor in automotive Inverter designs must be cooled and mounted on a heatsink. At best, the cooling fluid of a liquid cooled heatsink should pass the capacitor first before cooling the hot semiconductor switches, respecting temperature limits and magnitude of the absolute dissipation in Watts. Another consideration, when selecting a DC-Link capacitor, is the derating as a function of the applied temperature and voltage. Please check the data sheets or ask manufacturer for details.

Other considerations, besides the temperature, that need to be taken into account are humidity, vibration or even (chemical) contamination as already mentioned.

For instance, when including an EMI-Filter system into the inverter [5 MOD.INV/MIB] like TDKs CarXield™, also the filter needs cooling to achieve maximum continuous performance.

Calculating capacitor values
For the capacitor the load caused by the ripple current and the resulting ripple voltage is the first selection criterion. The ripple

$$I_{Crms} = \frac{\sqrt{3}}{\sqrt{2}} * m * \cos\varphi * I_{Mrms} = 1.22 * 0.5 * 0.8 * I_{Mrms} \approx 0.5 * I_{Mrms}$$

current that the capacitor must handle, without overheating by dissipation in the ESR (Equivalent Series Resistance), is often the overriding factor. In most cases, this leads to a capacitance, which is well over the minimum calculations.

Capacitor - Ripple Current I_{Crms}
The AC current flowing through the capacitors ESR causes the heating effect as follow:

Formula 1: Simplified calculation of capacitors rms current (I_{Crms})

Presumptions:

- I_{Mrms} (I_{Phx}) = Motor Phase Current in Ampere
- Cos ~ 0.8 (typical value)
- m = modulation index (worst case mentioned above) = 0.5

Example:

- I_{Mrms} = 250A

➔ I_{Crms} = 1.22 * 0.5 * 0.8 * 250A 0.5 * 250A = 125A

Nevertheless, for 3-phase systems, the following formula match better:

➔ I_{Crms} = 1.3 * I_{Mrms} / 2

Formula 2: Most used simplified calculation of capacitors rms current (I_{Crms})

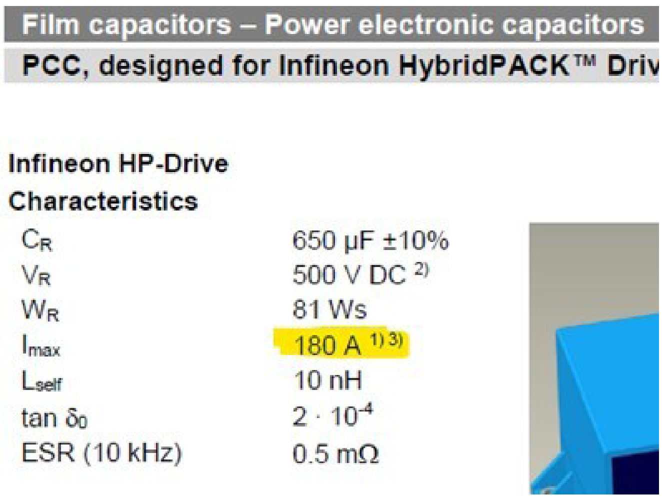

Figure 4: I_{Crms} with temperature restrictions

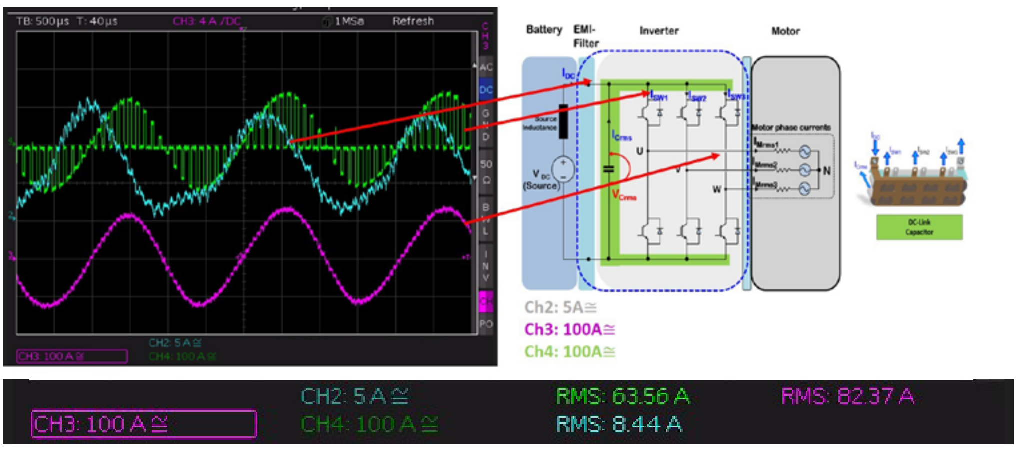

Figure 5: Measurements on an IFX HP-Drive module with a TDK film capacitor [Source: Mankel-Engineering.de]

Example:

➔ I_{Crms} = 1.3 * 250A * 0.5 = 1.3 * 125A = 162,5A

With these rough calculated capacitor ripple current, you can check in the capacitors data sheet (Figure 4), and determine which one may fit to your design to cover this value.

Figure 5 shows the example of a PWM inverter currents measurement.

The currents of **CH2** and **CH4** were each measured with a Rogowski coil and the measurement at **CH3** with an active AC/DC current clamp.

CH2 shows the current drawn from the DC supply, in this case the battery. The current amplitude has the frequency of the output frequency with a superimposed current ripple of the switching frequency. The current ripple depends on the DC link capacitance and the leakage inductance of the supply line.

CH3 shows the phase current with the ripple of the pulse width modulation. The current ripple mainly depends on the load inductance.

CH4 shows the current drawn by the pulse width modulation from the DC link capacitor in a half bridge. The current is driven into the load inductance by the pulse width modulation of the semiconductor switches, as well as the envelope of the output current.

In this case, when a special capacitor for the HP-Drive module is used, only the current per half bridge can be measured due to these specific connection conditions of the capacitor.

Capacitor - Ripple Voltage V_r
Explanation of used values in formulas - (Figure 6 (simplified) and 7).

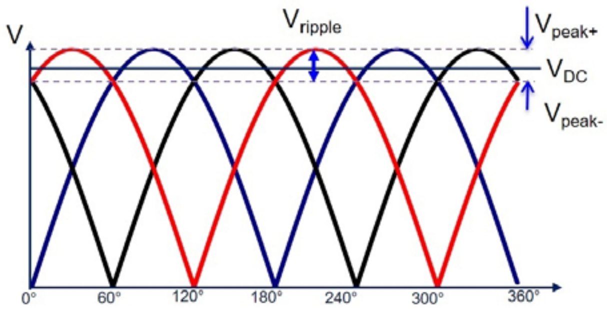

Figure 6: Simplified DC-link voltage switching ripple (Vr)
[4 Source: Rambow-Technology]
Rated Voltage (DC-Voltage) $V_R = V_{DC}$
Maximum Ripple Voltage $V_{ripple} = V_r = V_{pp} = V_{pkpk}$

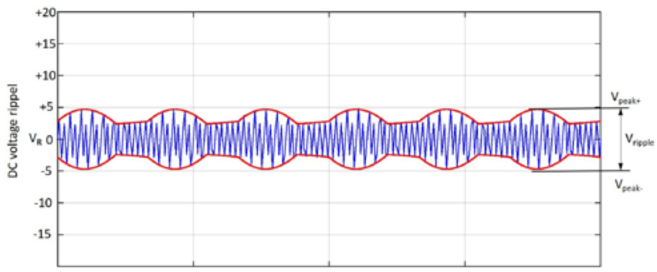

Figure 7: DC-link voltage switching ripple (Vr) - modified curve, results (blue trace) and calculated peak-to-peak Envelope (red trace) over time; m = 0.50
[4 Source: Curve modified by Rambow Technology]

$$V_{Crms} = V_{pk}\ x\ \frac{1}{\sqrt{2}} = V_{pk}\ x\ 0.7071$$

Formula 3: Simplified calculation of the Capacitor ripple voltage

If, for example, the OEM or Tier1 specify the ripple voltage (V_r) as +-12V, the peak voltage (V_{pk}) of the waveform is 12 V, but the ripple voltage is 24V.

$V_{Crms} = V_{pk}$ * 0.7071 = 12V x 0.7071 = 8.48 V

Capacitor - Capacitance
Calculating the capacitance C while stands for the frequency in Hertz (Hz) and for the period duration in seconds (s).

$$f = \frac{1}{\tau} \qquad \omega = 2 * \pi * f$$

Rearranging equations:

$$C * 2 * \pi * f = \frac{I_{Crms}}{V_{ripple}}$$

$$\frac{1}{2 * \pi * f * C} = \frac{V_{ripple}}{I_{Crms}}$$

Equation:

$$C = \frac{I_{Crms}}{2 * \pi * f * V_{rippel}}\ \text{uF}$$

Formula 4: Calculate capacitance value - expected to be most realistic!

Example:
V_R or V_{DC} = 400V
f=10kHz (10000Hz)
I_{Crms} = 180A
$V_{peak-peakk} = V_{ripple}$ = 8V
DC=m=0.5

Capacitance can be approximated by:

➔ $C = \frac{I_{CrmS}}{2*\pi*f*V_{ripple}} = \frac{180}{2*3.14*10*1000*8} = 358\text{uF}$

Power Dissipation
A DCLink capacitor will experience internal heating, which will increase as the frequency of the ripple current of the semiconductors increases. Based on above sample calculating the power capacitor losses with low ESR - e.g. ~0.5mOhm:

$P_C = I^2_{Crms} * R_{CESR}$

Formula 5: Capacitor Power Dissipation

P_C=180²A * 0.5mOhm = 32400 * 0.0005 = 16.2W

The following capacitance values for a 100kW inverter base on best practice expertise:
650uF for 450V systems ➔ Capacitor 650uF/500Vr
400uF for 800V systems ➔ Capacitor 400uF/855Vr

Do not forget - capacitors total heating and temperature rises depend on the following main factors:
- Self-heating
- DC-current on the bus-bars
- Heat Injection from the semiconductors (tabs)
- Cooling
- Time

Conclusion
Now you have calculated the needed capacitor values provisionally to choose the capacitor, but please keep in mind you are not finished. Measuring and evaluating your results in a final hardware environment of the device will validate your results and looking at the following Issues will help you to prevent unexpected thermal damages.

Issues
More capacitance will not decrease the ripple voltage
Looking to Figure 8 adding more capacitance than needed will not reduce the ripple voltage effectively. The allowable ripple voltage of ~12V will be achieved with ~350uF. A capacitance value between 500uF and 650uF seems to be a good solution handling the capacitor's ripple current. Spending more would not be cost effective.

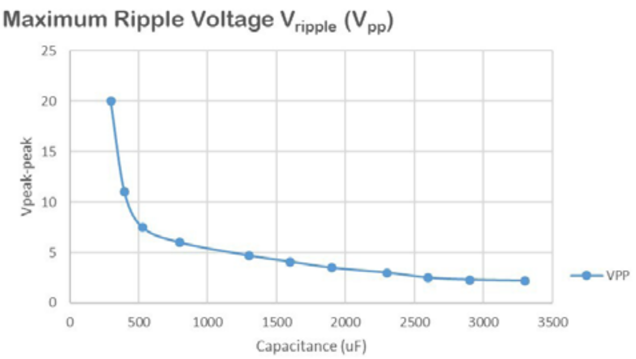

Figure 8: Example - Capacitance values versus ripple voltage [Source: Rambow-Technology]

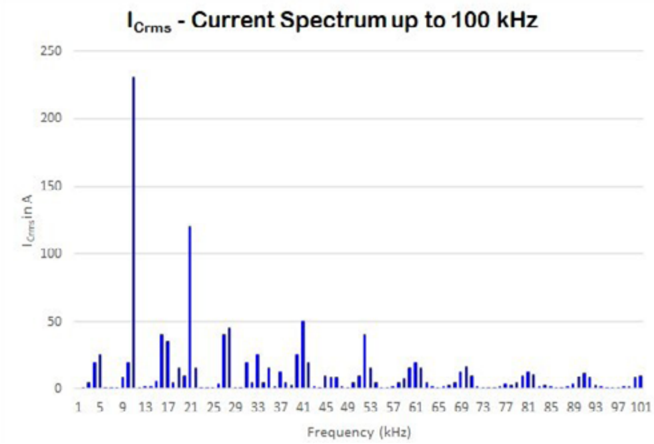

Figure 9: Amplitude of ICrms gaining losses up to 100 kHz [Source: Rambow-Technology]

Resonances causes capacitor losses
Resonance between capacitor and your switching circuitry lead to a wide frequency spectrum. Usually people like to stop measuring at 100 kHz for a 10 kHz inverter – such results are indicated in Figure 9 - which are seemingly good. However, you may be surprised when the capacitor fails "unexpectedly" due to temperature problems. The chart shows an analysis that obviously does not represent the performance of a well-designed inverter.

➔ Consider an extremely wide Frequency spectrum up to the MHz range (Figure 10)

With the use of "High Speed IGBTs" and even more with SiC wide bandgap semiconductors the switching frequency raises to 20 kHz and even more. On top, we have the inherently higher di/dt and dV/dt of these components compared with classical IGBT dedicat-

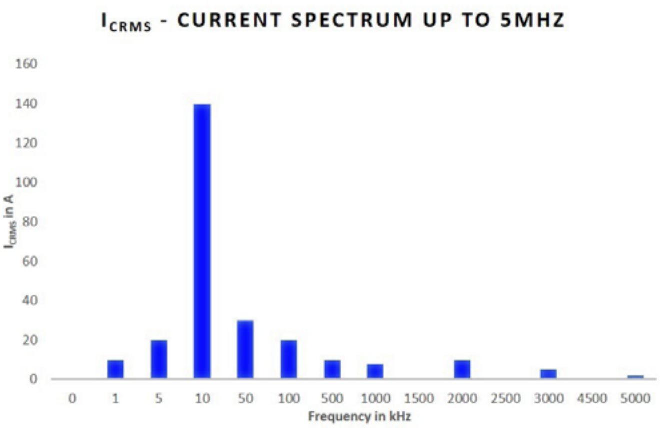

Figure 10: Amplitude of I_{Crms} gaining losses up to 5 MHz [Source: Rambow-Technology]

ed for motor control applications. Major losses produced by the semiconductor switching current relay on influence above 100 kHz. Consequently, it does not make any sense to consider an operation bandwidth only up to 100 kHz. At minimum it should cover all the harmonics from the PWM with a magnitude higher than 10% of the total I_{rms} (e.g. 300 kHz or even up to the MHz range).

What is critical here?

Example - looking at the ESR of a power film capacitor and how its losses (ESR) change over frequency:
ESR @10kHz ~ 1 x ESR according the datasheet
ESR@50kHz ~ 2 x ESR@10kHz
ESR@50kHz to 100kHz ~ 4 x ESR@10kHz
ESR@100Khz to 300kHz ~ 6 x ESR@10kHz

The truth is that with above-mentioned ratios the power losses of the DCLink capacitor will increase drastically. Remember:

$P_C = I^2_{Crms} * R_{CESR}$

➔ Capacitors ESR should be low within the entire relevant current spectrum bandwidth.

With some design efforts, the Capacitor manufacturer and you can reduce these effects drastically.

Nevertheless, there are still some other considerations:
- Even if you are experienced, it is not easy to estimate the complete spectrum in advance.
- All the shown harmonics depend on pulse with modulation (PWM) strategy and parameters set by you.
- DCLink capacitor in automotive inverters are strongly affected by the switching semiconductors and their transients plus possible ringing effects with high order harmonics that are difficult to predict.

The selection of a suitable capacitor is physically possible with classic electro technical approaches and requires a precise model of the parasitic of a power stage built with this capacitor. That is a difficult task by nature. However, experience and best practice results can significantly help to shorten design iterations. The in-depth analysis paired with state-of-the-art field results will be part of dedicated seminars like "Elektroauto (xEV) E-Motor + Antriebsumrichter 500V + 800V / IGBT und SiC" by www.mankel-engineering.de.

References
Since this article describes a long-term used product, most formulas and pictures are widely used as standard in lots of publications with no reference.

[1 https://www.ti.com/lit/an/slta055/slta055.pdf]

[2 https://www.electronics-tutorials.ws/de]

[3 Rohde&Schwarz Tutorial PWM: https://www.youtube.com/watch?v=nXFoVSN3u-E]

[4 Curve taken from Analysis of dc-Link Voltage Switching Ripple in Three-Phase PWM Inverters Marija Vujacic ID, Manel Hammami ID, Milan Srndovic ID and Gabriele Grandi * ID - page 11]

[5 Modular Inverter - MOD.INV/MIB by MankelEngineering.de ➔ Bodo's Power Systems magazine 10/2022 page 40]

[6source: TDK Data sheet Automotive Power Film Capacitor]

www.rambow-technolgy.com
www.mankel-engineering.de